MIPI CSI-2 IP Core

IP core(Tx/Rx) for FPGA which based on CSI-2 standard
Serial Data Transfer : Camera - Application Processer

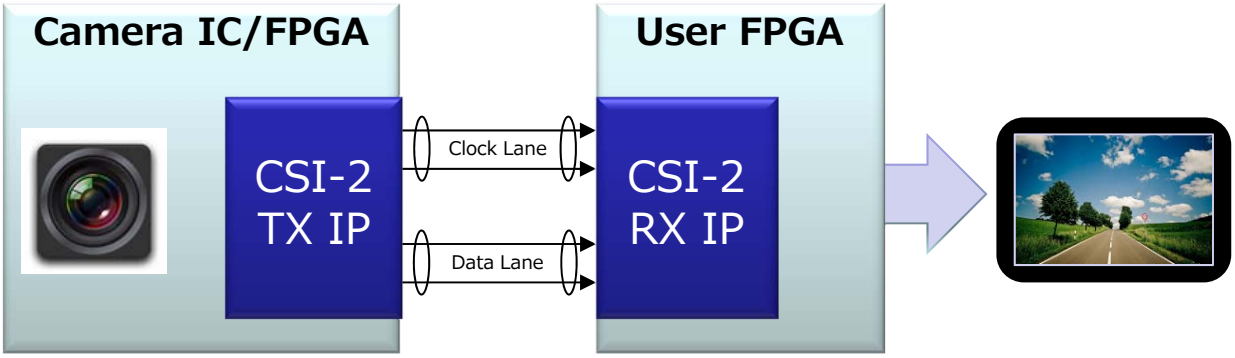
Characteristic

MIPI CSI-2(Tx/RX) I/F by FPGA

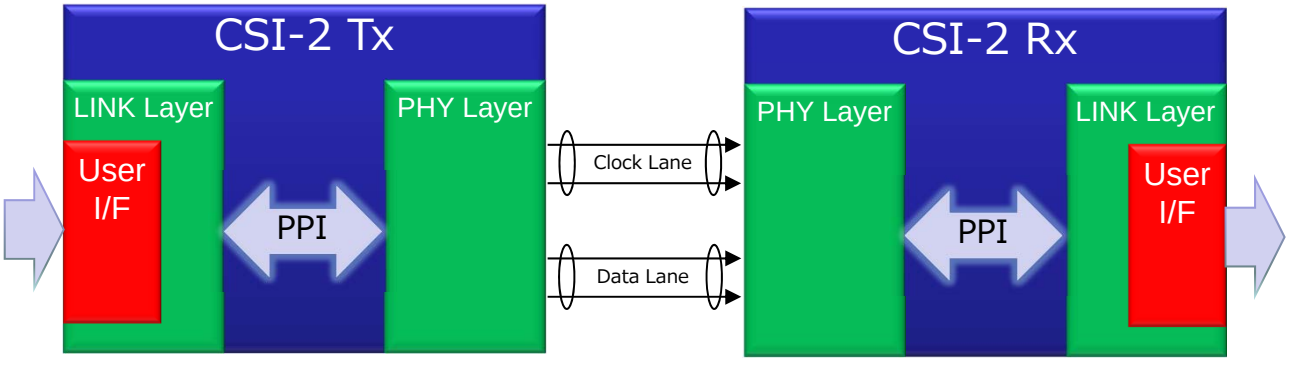
Merit of IP for FPGA	**Realize MIPI I/F with Low cost** ➢ **Series development for small quantity, large variety** ➢ **Available for evaluation of Product development**

Example of System

CSI-2 Tx : After Image processing in Camera IC, Output by MIPI CSI-2 Tx
CSI-2 Rx : Receive Camera IC data in CSI-2 Rx, Output to Display after image processing.



Customize



IP core customization according to customer needs.(User I/F、output through MIPI)
This IP has PPI(Phy Protocol I/F) and, it's possible to supply either LINK Layer or PHY Layer.

Specifications

Main Specification of CSI-2 IP Core

	CSI-2 TX	CSI-2 RX
Standard	mipi alliance CSI-2 v1.1 / v1.0100	mipi alliance CSI-2 v1.1 / v1.0100
	mipi alliance DPHY v1.1	mipi alliance DPHY v1.1
Clock Lane	1Lane	1Lane
Data Lane	1Lane ～ 4Lane	1Lane ～ 4Lane
Clock Mode	Continuous	Continuous Only
	Non-Continuous	
Bit Rate	Max 800Mbps / Lane ※1	Max 800Mbps / Lane ※1
Data Formats	RAW8,RAW10,RAW12,RAW14	RAW6,RAW7,RAW8,RAW10,RAW12,RAW14
	RGB565,RGB666,RGB888	RGB444,RGB555,RGB565,RGB666,RGB888
	YUV422(8bit,10bit)	Legacy YUV420(8bit),YUV420(8bit,10bit),YUV422(8bit,10bit)
	Embedded 8-bit non Image Data	Embedded 8-bit non Image Data
	User Defined Byte-based Data	User Defined Byte-based Data
	NULL、Blanking Data	NULL、Blanking Data
Escape Mode	Ultra-Low Power State(ULPS) Only	Ultra-Low Power State(ULPS) Only

※1 Maximum bit rate is according to device classification.

CSI-2 IP core FPGA Resorce

Cyclone V Result	CSI-2 Tx	CSI-2 Rx
Logic utilization(in ALMs)	2,200	2,800
Total registers	2,300	2,700
Total block memory bits	115K	0
Total PLLs	2	1
Total DSP Blocks	0	0

※Depending on a request, we cope with the MAX10/Cyclone/Arria/ other series.

Deliverable

Deliverable List

- **RTL or Netlist**
- **IP functional specification sheet**
- **IP deaign specification sheet**
- **IP verification environment(sample pattern)**

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