June 9, 2016
Shikino High-Tech Co., Ltd.

Shikino Launches the FPGA Version of IP for Full HD Videos

("World-smallest class" still image compression/ decompression IP and High-speed interface IP)

UOZU (June 9, 2016) —Shikino High-Tech Co., Ltd. ("Shikino") today announced that it has launched 3 new products (codec IP, encoder IP and decoder IP) from "KJN-F4", a Shikino's new product line featuring the FPGA[1]* version of the still image compression/decompression IP with the world's top share (the KJN series for JPEG IP), and 2 new products (RX IP and TX IP) from "MIPI CSI-2 IP", another new product line of the high-speed FPGA interface IP. It commenced its sales on June 8, 2016.
"KJN-F4 IP" enables users to compress and decompress full high vision images at 30 fps. "MIPI CSI-2 IP" complies with MIPI, the image sensor interface standard, and is most suitable for the industrial devices centering on the surveillance/ medical/ automotive fields and so forth due to the effectiveness to be mounted on FPGA.

[1]*FPGA: Field-programmable gate array. It is a kind of integrated circuits and, unlike a dedicated SoC[2]*, a general-purpose LSI that can be updatable by rewriting programs after being shipped to customers. A FPGA is widely used for the industrial purposes that frequently demand small quantity and large variety since users are able to purchase it even from a single unit.

[2]*SoC: System on a chip. It is not a single LSI but an integrated circuit that integrates the whole system including hardware and software such as digital and analog circuits having microcontrollers and software into a single chip.

◆Overview

Higher sensitivity and resolution in images have been progressed in the industrial purposes such as security cameras and inspection equipment, and image data volumes to be processed have increased. Following this technological advance, the increasing demand for higher speed process of a large amount of data is growing even further. A dedicated SoC used to be employed frequently to process a large amount of data with high speed and it had been one of the issues in terms of cost for the industrial purposes demanding small quantity and large variety regularly.
As a solution of the abovementioned issue, Shikino developed "KJN-F4", an optimized high-speed still image compression/ decompression IP for FPGA, and "MIPI CSI-2 IP", a high-speed interface IP. These products were launched as Shikino's first FPGA lineup.
In anticipation of the market expansion in FPGA ranging from consumer electronic products, broadcasting equipment, medical devices to automotive devices and the diversification of customer needs, Shikino will expand product lineups of FPGA JPEG IP products (the KJN-F series) and high-speed interface IP products focusing on the business-to business (B2B) market.

◆Features (KJN-F4)

●Small-scale and low power consumption

Minimize gate amounts and reduce 45% of the power consumption by our original implementing technology in comparison with our conventional products.

●High performance

Process full high definition images at 30 fps with this low-cost FPGA device.

●High reliability

Optimize our existing IP with abundant market experience in smartphones and DSC for FPGA.

●Various product lineups

Provide three products: Codec IP, encoder IP and decoder IP.

◆Applications

Monitoring instruments, medical devices, automotive devices, aerospace instruments and OA equipment.

Specifications (KJN-F4)

- CPU bus : 32 bits
- Image data bus : 32 bits
- Code data bus : 32 bits
- Quantization table : 4 tables (RAM)
- Huffman table : 2 tables for DC and AC respectively (Fixed)
- Color format : YUV444, YUV422, YUV420, YUV411, Gray-Scale and CMYK

◆Features (MIPI CSI-2 IP)

●Small-scale and low cost

Optimize circuits as a FPGA version of IP in accordance with the separate connection method of MIPI high speed signals and low speed signals recommended by FPGA manufacturers and connect the image sensor to FPGA directly.

●High performance

Process full high definition images at 30 fps with this low-cost FPGA device.

●High reliability

Newly developed MIPI CSI-2 IP as a FPGA version of IP by making use of our technology with

abundant experience in the SoC development.

●Support various image data formats
Support RAW, RGB and YUV.

●Product lineups
Provide two products: RX (Receiver) IP and TX (Transmitter) IP.

◆Applications (MIPI CSI-2 IP)

Inspection equipment, monitoring instruments, medical devices, automotive devices and OA equipment.

Specifications (MIPI CSI-2 RX IP[SHSA0001]/ TX IP[SHSA0002])

- Applicable standard : MIPI Alliance CSI-2 v1.1/ v1.0100 and D-PHY v1.1
- Clock lane : 1 lane
- Data lane : 1-4 lanes
- Bit rate : 500Mbps/Lane (Maximum 2.0Gbps with 4 lanes in total)
  Note: This rate varies depending on the FPGA devices to be used.
- Data format : RAW6*, RAW7*, RAW8, RAW10, RAW12, RAW14, RGB444*, RGB555*, RGB565, RGB666, RGB888, Legacy YUV420 (8 bits)*, YUV420 (8 bits and 10bits)*, YUV422 (8 bits and 10 bits), Embedded 8-bit non Image Data, User Defined Byte-based Data, NULL and Blanking Data (*Applicable only for RX)
- Escape mode : Applicable only for Ultra-Low Power State (ULPS)

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